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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,419	10/26/2000	Alan McNutt	99 P 7938 US 01	5374

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Elsa Keller
SIEMENS CORPORATION
Intellectual Property Dept.
186 Wood Avenue South
Iselin, NJ 08830

EXAMINER
VU, TUAN A

ART UNIT	PAPER NUMBER
2124	11

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _26 March 2004_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under _Ex parte Quayle_, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _4-11(1-3 cancelled)_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _4-11_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This action is responsive to the Applicant's response filed 3/26/2004.

As indicated in Applicant's response, claims 1-3 have been canceled and claims 4-11

added. Claims 4-11 are pending in the office action.

Claim Objections

2.   Claims 4,5, 7, 9 and 11 are objected to because of the following informalities: the

element recited as 'support kernal' (line 7, 11, 6, 6, 11, respectively) needs to be corrected to

become 'support kernel'. Appropriate correction is required.

3.   Claims 5, 7, 9, and 11 are objected to because there is inconsistency between the

limitations recited as 'binary programmable logic controller program' and 'binary programmable

logic control program'. For example, claim 5, line 7 limitation 'said binary programmable logic

control program' should be adjusted to be 'binary programmable logic controller program'.

Inconsistencies similar are in claim 7, line 7, where 'said binary programmable logic controller

program' should be the other 'said binary programmable logic control program', in claim 9, line

6 and claim 11, line 7. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

5.   Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing

to particularly point out and distinctly claim the subject matter which applicant regards as the

invention.

As per claim 7, there is no connecting term between elements 'said binary programmable

logic control program' and 'a compilation of a symbol...'; making the relationship between the 2

elements unclear. Examiner will treat this as if such control program were derived from the

'compilation ...'. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

7.   Claims 4-9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Agrawal et al., USPN: 5,179,716 (hereinafter Agrawal), in view of Gates, USPN: 4,969,083 (

hereinafter Gates)), and further in view of Kaiser et al., USPN: 4,527,247 (hereinafter Kaiser).

As per claim 4, Agrawal discloses a programmable logic controller (PLC), said PLC

comprising:

a single chip program execution device comprising a microcontroller operable to

implement the PLC I/O operations upon executing compiled user program instructions (e.g. col.

1, lines 20-24; Fig. 1; Fig. 2; col. 3, lines 9-63); and

a re-programmable read-only memory within which compiled is stored (e.g. Fig. 5;

EPROM -col. 19, lines 2-6);

But Agrawal does not explicitly disclose that implementing said PLC I/O functions is

from a compilation comprising a support kernel. But in view of Agrawal's teachings as to be

able to initialize the power settings or memory or power-up of the controller (e.g. col. 18, lines

32-45; Fig. 1), such kernel related support instructions is implicitly disclosed because of the

must-have nature of kernel support in every system being programmed for actualizing its very

functionality, i.e. I/O communications instructions as in Agrawal's case.

Nor does Agrawal explicitly disclose that said single chip program execution device is

separable from a communication/programming device adapted to compile the user program;

even though Agrawal discloses that instructions are controlled by user's specifications (e.g. Fig.

2; col. 3, lines 20-28), which suggests that the PLC does not come with a built-in compiler.

Having a external device for providing interface and compilation resources for controlling the

basic operating system and actualizing the functionality of a programmable controller was a

known concept at the time the invention was made. For example, in a method to program a PLC

performing a ladder logic control, Gates discloses this external communication device adapted

for compiling the programmable functionality of the PLC (e.g. *PC 11* -Fig. 2). In case

Agrawal's system does not already teach such external communication device for effecting the

compilation of the PLC's program, it would have been obvious for one of ordinary skill in the art

at the time the invention was made to provide such external compiling device as taught by Gates

to Agrawal's system because the single-chip controller by its very inception and architecture as

taught by Agrawal is not designed basically for performing a compilation/debug of high-level

code but merely adapted to execute translated instructions provided to its execution resources as

intended by Agrawal; and providing such external device would alleviate resources from the

PLC.

Nor does Agrawal disclose that the PLC as not having a memory device external to said

single chip. The I/O dynamically alterable system by Agrawal can be expanded to communicate

with external memory (e.g. *can be programmed* - col. 15, lines 41-47); but because it is flexible,

this external memory feature can be lacking. Further, in a system to use programmable memory

to store program instructions to actualize a controller analogous to that of Agrawal or Gates,

Kaiser discloses the possibility to leave out the external memory connections when the supplied

EPROM is self-sufficient without further latching (e.g. *to obviate the need to latch* - col. 5 line

63 to col. 6, line 13). In case the EPROM in Agrawal's flexible connectivity system is

sufficiently supplied to behave as suggested by Kaiser, it would have been obvious for one of

ordinary skill in the art at the time the invention was made to leave out connectivity of the PLC

memory to external memories as suggested by Kaiser for the same rationale as taught by Kaiser.

As per claim 5, Agrawal discloses a method for

receiving a symbolic user program at a single-chip program execution device (Fig. 1),

said single chip device adapted to execute binary programmable logic controller (PLC) program

(e.g. col. 1, lines 20-24; Fig. 1; Fig. 2; col. 3, lines 9-63); such program stored in re-

programmable memory (Fig. 5; *EPROM* -col. 19, lines 2-6), and adapted to operate such PLC

(col. 3, lines 9-63).

But Agrawal does not explicitly disclose compiling to form said binary programmable

logic control program; however, Agrawal teaches user program being instructions to be loaded

for execution and having field controlled by the user(e.g. Fig. 2; col. 3, lines 20-28); and this

discloses that limitation because of the inherent nature of instructions being compiled for

execution. Agrawal fails to explicitly disclose a separate communication/programming device

for providing the compilation and the symbolic user program for the PLC single-chip execution

device. But this limitation has been addressed in claim 4 above.

Nor does Agrawal expressly disclose the kernel support being also provided with the

compilation of the user program to form the binary programmable logic control program; this

feature has been addressed in claim 4 above.

Nor does Agrawal disclose that the PLC is lacking a memory device separate from the

single-chip execution device; but this limitation has been addressed in claim 4 above.

As per claim 6, see Agrawal (Fig. 2; col. 3, lines 9-63).

As per claim 7, Agrawal discloses a method comprising: receiving a binary

programmable logic control program at a single-chip execution device (col. 1, lines 20-24)

having a re-programmable memory (Fig. 5; *EPROM* -col. 19, lines 2-6), said binary control

program being derived from a compilation of a symbolic user program (e.g. col. 3, lines 9-63),

said single-chip execution device adapted to execute said binary program to operate a PLC (col.

3, lines 9-63); loading said binary programmable logic control program into said programmable

memory (e.g. Fig. 5; PROM microinstructions - col. 11-14; *EPROM* -col. 19, lines 2-6).

Agrawal fails to explicitly disclose a separate communication/programming device for

providing the compilation and the symbolic user program for the PLC single-chip execution

device. But this limitation has been addressed in claim 4 above.

Nor does Agrawal expressly disclose the kernel support being also provided with the

compilation of the user program to form the binary programmable logic control program; this

feature has been addressed in claim 4 above.

Nor does Agrawal disclose that the PLC is lacking a memory device separate from the

single-chip execution device; but this limitation has been addressed in claim 4 above.

As per claim 8, see Agrawal (Fig. 1; col. 3, lines 9-63).

As per claim 9, Agrawal discloses a programmable logic controller system, comprising:

a single-chip execution device (col. 1, lines 20-24) having a re-programmable memory

(Fig. 5; *EPROM* -col. 19, lines 2-6) storing a binary programmable logic controller program, said

program executed by said execution device;

said programmable logic program comprising a compilation of user program and system

support (Fig. 1; col. 3, lines 9-63; col. 11-14);

said program adapted to operate a PLC (col. 3, lines 9-63); said binary programmable

logic controller program being stored in said re-programmable memory by direct manipulation of

logic controls of said re-programmable memory (Fig. 5; PROM microinstructions - col. 11-14;

EPROM -col. 19, lines 2-6)

Agrawal fails to explicitly disclose a separate communication/programming device for

providing the compilation, communicating and loading of said binary program into said memory

of said single-chip execution device. These limitations are explicitly or implicitly disclosed in

Gates as addressed in claim 4 above; and are also obvious in light of such rationale.

Nor does Agrawal expressly disclose the kernel support being also provided with the

compilation of the user program to form the binary programmable logic control program; this

feature has been addressed in claim 4 above.

Nor does Agrawal disclose that the PLC is lacking a memory device separate from the

single-chip execution device; but this limitation has been addressed in claim 4 above.

As per claim 11, this is a computer-readable medium version of claim 7, hence is

rejected with the corresponding rejection as set forth in claim 7.

8.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al.,

USPN: 5,179,716, in view of Gates, USPN: 4,969,083 and Kaiser et al., USPN: 4,527,247, as

applied to claim 9, and further in view of McNutt, USPN: 5,802,389 (hereinafter McNutt).

As per claim 10, Agrawal discloses PLC functions via instructions for timing/clocking

events or synchronizing (e.g. col. 6, lines 30-42) and multiplexing signals or pipelining

instructions (e.g. timing is complete - col. 13-14; Fig. 12-15) but does not expressly disclose a

watchdog timer. The control of parallel signals coming to and going from a system under the

control for a PLC suggests the use of timer like the watchdog timer; and this is evidenced in the

system by McNutt, who, in a system using a PLC to control flow of data between registers and

bus lines to devices under monitoring analogous to the signal synchronizing by Agrawal,

discloses a watchdog timer service (col. 8, lines 40-55). It would have been obvious for one of

ordinary skill in the art at the time the invention was made to provide to the PLC system by

Agrawal the watchdog timer service or hardware as suggested by McNutt because controlling the

concurrent signal in and out of a PLC-controlled system requires a timer so as to ascertain bus

privileges or usability, or access priorities so to avert collision or resources contentions/clashes

so well known in the purpose of using watchdog timer.

Response to Arguments

9.   Applicant's arguments filed 3/26/2004 have been fully considered but they are not

persuasive.

Applicant has submitted that Gates teaches a 'multitasking ... shell' and does not teach or

suggest a 'communication/programming ... system support kernel" (Appl. Rmrks, pg. 8, 4th

para). In response, Examiner likes to point out that from the current rejection, Gates does

provide a external device to ensure code compilation and downloading into the memory

resources of the controller executing environment. The element of 'kernel support' might not be

explicitly disclosed, but in view of the programmable code logic being built and loaded for

executing the very functionality of Gates's PLC or Agrawal's PLC, e.g. I/O communications or

debug/emulation signaling functions which the PLC is purported to deliver, the concept of

support for boot-up, initializing remisniscent of kernel support or execution at low-level layer

software prior to the higher-level controller routine functions is strongly implied. Moreover, the

Gates is mainly to address the lacking communication device in Agrawal's system and is not

intended for addressing the kernel feature, which is considered as implied in Agrawal's (see

claim 4).

The rest of Applicant's arguments are moot in view of the currently submitted rejection

which is necessitated by the amendments.

Conclusion

10.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The

examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please consult Examiner

before using this number)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,

Arlington. VA. , 22202. 4th Floor(Receptionist).

Information regarding the status of an application may be obtained from the Patent

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VAT
May 21, 2004